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**EDUCATION**

**Ph.D In Computer Engineering**Sharif University of Technology 2006-2010
**M.Sc In computer engineering**Sharif University of Tehnology 2003-2006
**B.Sc In computer engineering**Amirkabir University of Tehnology 1999-2003

**PUBLICATIONS**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **761** | **15** | **25** | **35** | **8** |
| Citations | h-Index | Article | Conference | Book |

***Articles***

**1.** Reconfigurable Network-on-Chip based Convolutional Neural Network Accelerator. Firuzan Arash, Modarressi Mehdi, reshadi media, Ahmad Khademzadeh (2022)., JOURNAL OF SYSTEMS ARCHITECTURE, 129(1), 102567.

**2.** Energy-efficient acceleration of convolutional neural networks using computation reuse. Ghanbari Azam, Modarressi Mehdi (2022)., JOURNAL OF SYSTEMS ARCHITECTURE, 126(1), 102490.

**3.** Efficient photodetector placement for daylight-responsive smart indoor lighting control systems. Seyedolhosseini Atefesadat, Modarressi Mehdi, Masoumi Nasser, Karimiyan Noshin (2021)., JOURNAL OF BUILDING ENGINEERING, 42(103031), 103013.

**4.** Daylight adaptive smart indoor lighting control method using artificial neural networks. Seyedolhosseini Atefesadat, Masoumi Nasser, Modarressi Mehdi, Karimiyan Noshin (2020)., JOURNAL OF BUILDING ENGINEERING, 29(ISSN: 2352-7102 101141), 101141.

**5.** ΔNN: Power-efficient Neural Network Acceleration using Differential Weights. Mahdiani Hoda, Khadem Alireza, Ghanbari Azam, Modarressi Mehdi, Fatahi Bayat Farima, masoud daneshtalab (2020)., IEEE Micro, 40(1), 1-1.

**6.** NoM: Network-on-Memory for Inter-Bank Data Transfer in Highly-Banked Memories. SeyyedAghaei Rezaei Seyyed Hossein, Modarressi Mehdi, Ausavarungnirun Rachata, Mutlu Onur, Sadrosadati Mohammad, Masoud Daneshtalab (2020)., IEEE Computer Architecture Letters, 19(1), 80-83.

**7.** A memory architecture to accelerate data movement inside memory. Dabiri Bita, Modarressi Mehdi (2019)., The CSI Journal on Computing Science and Information Technology, 1(1), 1-7.

**8.** BARAN: Bimodal Adaptive Reconfigurable-Allocator Network-on-Chip. Mirhosseini Amirhossein, Sadrosadati Mohammad, aghamohamadi fatemeh, Modarressi Mehdi, Sarbazi-azad Hamid (2019)., ACM Transactions on Parallel Computing, 5(3), 1-29.

**9.** Fast Data Delivery for Many-Core Processors. Bakhsalipoor Mohamad, Lotfi Kamran Pejman, Mazloumi Abbas, Samandi Farid, Naderan-Tahan Mahmood, Modarressi Mehdi, Sarbazi-Azad Hamid (2018)., IEEE TRANSACTIONS ON COMPUTERS, 67(10), 1416-1429.

**10.** Thermal management in 3d networks-on-chip using dynamic link sharing. Keramati Mahsa, Modarressi Mehdi, Seyedaghaei Rezaei S. Hossein (2017)., MICROPROCESSORS AND MICROSYSTEMS, 52(1), 69-79.

**11.** Fault-Tolerant 3-D Network-on-Chip Design using Dynamic Link Sharing. Seyedaghaei Rezaei S. Hossein, Modarressi Mehdi (2017)., rayanesh, 6(1), 1-7.

**12.** Customizing Clos Network-on-Chip for Neural Networks. Hojabrossadati Seyedreza, Modarressi Mehdi, Daneshtalab Masoud, Yasoubi Ali, Khonsari Ahmad (2017)., IEEE TRANSACTIONS ON COMPUTERS, pp(99), 1-1.

**13.** Power-Efficient Accelerator Design for Neural Networks Using Computation Reuse. Yasoubi Ali, Hojabrossadati Seyedreza, Modarressi Mehdi (2017)., IEEE Computer Architecture Letters, 16(1), 72-75.

**14.** An Efficient Hybrid-Switched Network-on-Chip for Chip Multiprocessors. Pejman Lotfi Kamran, Modarressi Mehdi, Sarbazi-azad Hamid (2016)., IEEE TRANSACTIONS ON COMPUTERS, 65(5), 1-1.

**15.** Power- and performance-efficient cluster-based network-on-chip with reconfigurable topology. Mehrvarzi Pooyan, Modarressi Mehdi, h Sarbazi-Azad (2016)., MICROPROCESSORS AND MICROSYSTEMS, online(online), 1-14.

**16.** high-performance and low-power NoC for neurla networks. اکبری نسرین, Dabiri Bita, Modarressi Mehdi (2016)., The CSI Journal on Computing Science and Information Technology, 13(2), 60-69.

**17.** Dynamic Resource Sharing for High-Performance 3-D Networks-on-Chip. Seyyedaghaei Rezaei Seyyed Hossein, Mazloumi Abbas, Modarressi Mehdi, Lotfi Kamran Pejman (2016)., IEEE Computer Architecture Letters, 15(1), 5-8.

**18.** Leveraging dark silicon to optimize networks-on-chip topology. Modarressi Mehdi, Sarbazi-azad Hamid (2015)., JOURNAL OF SUPERCOMPUTING, 71(9), 3549-3566.

**19.** Improving the performance of packet-switched networks-on-chip by SDM-based adaptive shortcut paths. Modarressi Mehdi, Teimouri Nasibeh, Sarbazi-azad Hamid (2015)., INTEGRATION-THE VLSI JOURNAL, 50(Special Issue on OCPNBS), 193-204.

**20.** Integrated circuit-packet switching NoC with efficient circuit setup mechanism. Pakdaman Farhad, Mazloumi Abbas, Modarressi Mehdi (2014)., JOURNAL OF SUPERCOMPUTING, 71(8), 2787-2807.

**21.** Special issue on network-based many-core embedded systems. Daneshtalab Masoud, Liljeberg Pasi, Modarressi Mehdi, Soreas Leonardo (2013)., JOURNAL OF SYSTEMS ARCHITECTURE, 59(9), 691-692.

**22.** Using task migration to improve non-contiguous processor allocation in NoC-based CMPs. Modarressi Mehdi, Asadinia Marjan, Sarbazi-azad Hamid (2013)., JOURNAL OF SYSTEMS ARCHITECTURE, 59(7), 468-481.

**23.** Supporting non-contiguous processor allocation in mesh-based chip multiprocessors using virtual point-to-point links. Asadinia Marjan, Modarressi Mehdi, Sarbazi-azad Hamid (2012)., IET Computers and Digital Techniques, 6(5), 302-317.

**24.** Application-Aware Topology Reconfiguration for On-Chip Networks. Modarressi Mehdi, Tavakol Arash, Sarbazi-azad Hamid (2011)., IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 19(11), 2010-2022.

**25.** Virtual Point-to-Point Connections for NoCs. Modarressi Mehdi, Tavakol Arash, Sarbazi-azad Hamid (2010)., IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, 29(6), 855-868.

***Books***

**1.** Power-Efficient Network-on-Chips: Design and Evaluation. Modarressi Mehdi, SeyyedAghaei Rezaei Seyyed Hossein (2022).

**2.** Power-Efficient Network-on-Chips: Design and Evaluation. Sadrosadati Mohammad, Mirhosseini Amirhossein, akbarzadeh negar, Modarressi Mehdi, Sarbazi-azad Hamid (2022).

**3.** Hardware Architectures for Deep Learning. Hojabr reza, Khonsari Ahmad, Modarressi Mehdi, Daneshtalab Masoud (2020).

**4.** Hardware Architectures for Deep Learning- Ch1. masoud daneshtalab, Modarressi Mehdi (2020).

**5.** Hardware Architectures for Deep Learning. Mahdiani Hoda, Khadem Alireza, Yasoubi Ali, Ghanbari Azam, Modarressi Mehdi, m daneshtalab (2020).

**6.** Advances in Computers: Dark Silicon and Future On-chip Systems. Modarressi Mehdi, Sarbazi-azad Hamid (2018).

**7.** Routing Algorithms in Networks On-Chip. Modarressi Mehdi, Sarbazi-azad Hamid, Jabbarvand Reyhane (2013).

**8.** Large scal network centric distributed systems. Modarressi Mehdi, Sarbazi-azad Hamid (2013).

***Conferences***

**1.** Multi-Precision Deep Neural Network Acceleration on FPGAs. Neda Negar, Ullah Salim, Mahdiani Hoda, Ghanbari Azam, Modarressi Mehdi, Kumar Akash (2022)., 2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC), 17-20 January, Taipei, Taiwan.

**2.** Network-on-ReRAM for Scalable Processing-in-Memory Architecture Design. Dabiri Bita, Modarressi Mehdi, Masoud Daneshtalab (2021)., 2021 24th Euromicro Conference on Digital System Design (DSD), 1-3 September.

**3.** RoCo-NAS: Robust and Compact Neural Architecture Search. Geraeinejad Vahid, Sinaeei Sima, Modarressi Mehdi, Masoud Daneshtalab (2021)., 2021 International Joint Conference on Neural Networks (IJCNN), 18-22 July.

**4.** Zone Based Control Methodology of Smart Indoor Lighting Systems Using Feedforward Neural Networks. Seyedolhosseini Atefesadat, Masoumi Nasser, Modarressi Mehdi, Karimiyan Noshin (2018)., 9th International Symposium on Telecommunications (IST2018), 17-19 December, Tehran, Iran.

**5.** Design and Implementation of Efficient Smart Lighting Control System with Learning Capability for Dynamic Indoor Applications. Seyedolhosseini Atefesadat, Masoumi Nasser, Modarressi Mehdi, Karimiyan Noshin (2018)., 9th International Symposium on Telecommunications (IST2018), 17-19 December, Tehran, Iran.

**6.** Reconfigurable Network-on-Chip for 3D Neural Network Accelerators. Firuzan Arash, Modarressi Mehdi, masoud daneshtalab, Reshadi Midia (2018)., 12th IEEE/ACM International Symposium on Networks-on-Chip, 4-5 October, Torino, ITALY.

**7.** A Customized Processing-in-Memory Architecture for Biological Sequence Alignment. Akbari Nasrin, Modarressi Mehdi, masoud daneshtalab, Loni Mohamad (2018)., 29th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors, 10-13 July, Milan, ITALY.

**8.** NOC characteristics of cloud applications. Lotfi Kamran Pejman, Modarressi Mehdi, Sarbazi-azad Hamid (2017)., 19th International Symposium on Computer Architecture and Digital Systems (CADS), 21-23 December, IRAN.

**9.** Performance Improvement of ZigBee Networks in Coexistence of Wi-Fi Signals. Seyedolhosseini Atefesadat, Masoumi Nasser, Modarressi Mehdi (2017)., 7th International Conference on Information Communication and Management, 28-30 August, Russia.

**10.** Low-power Parallel Data Processing Using Computation Reuse. Dabiri Bita, Seyedaghaei Rezaei S. Hossein, Modarressi Mehdi (2017)., 7th International Conference on Information Communication and Management, 28-30 August, Russia.

**11.** A High-Performance Network-on-Chip Topology for Neuromorphic Architectures. Akbari Nasrin, Modarressi Mehdi (2017)., 15th IEEE International Conference on Embedded and Ubiquitous Computing (EUC), 21-24 July, China.

**12.** SAMi: Self-aware migration approach for congestion reduction in NoC-based MCSoC. Rezaei Amin, Daneshtalab Masoud, Zhao Dan, Modarressi Mehdi (2017)., 29th IEEE International System-on-Chip Conference (SOCC), 24-25 April, United States.

**13.** Parallel Forwarding for Efficient Bandwidth Utilization in Networks-on-Chip. Momenzadeh Elham, Modarressi Mehdi, Mazloumi Abbas, masoud daneshtalab (2017)., 30th International Conference on Architecture of Computing Systems, 3-6 April, Austria.

**14.** Near-Ideal Networks-on-Chip for Servers. Lotfi Kamran Pejman, Modarressi Mehdi, Sarbazi-azad Hamid (2017)., 23rd International Symposium on High Performance Computer Architecture (HPCA23), 4-6 February, United States.

**15.** Low-Power Online ECG Analysis Using Neural Networks. Modarressi Mehdi, Yasoubi Ali, Modarressi Maryam (2016)., 19th Euromicro Conference on Digital System Design (DSD), 31 August-2 September, Cyprus.

**16.** Proactive Network-on-Chip Path Setup for Message Passing Programs. Azimi Mohammad, Modarressi Mehdi (2016)., 19th EuroMicro Conference on Digital System Design (DSD), 31 August-2 September, Cyprus.

**17.** High Performance Hybrid-switched Network-on-Chip Using Shortcut Paths. Sayyardoust Tabrizi Sina, Soltani mohammadi Iman, Mazloumi Abbas, Modarressi Mehdi (2016)., 24th Iranian Conference on Electrical Engineering (ICEE), 10-12 May, Iran.

**18.** Fault-Tolerant 3-D Network-on-Chip Design using Dynamic Link Sharing. Seyedaghaei Rezaei S. Hossein, Modarressi Mehdi, Yazdani Aminabadi Reza, masoud daneshtalab (2016)., Design, Automation and Test in Europe Conference (DATE), 14-18 March, Germany.

**19.** low-power tag for compressed cache. Sayyardoust Tabrizi Sina, Modarressi Mehdi (2016)., 21th CSI conference, 8-10 March, Tehran, IRAN.

**20.** low power cache design for embedded systems using tag compression. Sayyardoust Tabrizi Sina, Modarressi Mehdi (2016)., 21 the CSI Computer Conference, 8-10 March, Iran.

**21.** A Three-Dimensional Networks-on-Chip Architecture with Dynamic Buffer Sharing. Seyedaghaei Rezaei S. Hossein, Modarressi Mehdi, Daneshtalab Masoud, Roshani Sefat Shervin (2016)., 24th Euromicro International Conference on Parallel, Distributed and Network-Based Processing., 17-22 February, Greece.

**22.** CuPAN – High Throughput On-chip Interconnection for Neural Networks. Yasoubi Ali, Hojabrossadati Seyedreza, Takshi Hengameh, Modarressi Mehdi, masoud daneshtalab (2015)., 22nd International Conference of Neural Information Processing (ICONIP), 9-12 November, Turkey.

**23.** Hardware Accelerator Protein Sequencing Applications on Reconfigurable Networks-on-Chip. Modarressi Mehdi, Faghih Faezeh, Modarressi Maryam (2015)., 13th. East-West Design and Test Symposium (EWDTS), 26-29 September, Georgia.

**24.** Process Variation-Aware Approximation for Efficient Timing Management of Digital Circuits. Faryabi Mohsen, Dorosti Hamed, Modarressi Mehdi, Fakhrai Seyed Mahdi (2015)., 13th IEEE East-West Design & Test Symposium (EWDTS), 26-29 September, Georgia.

**25.** Reconfigurable Communication Fabric for Efficient Implementation of Neural Networks. Firuzan Arash, Modarressi Mehdi, daneshtalab masoud (2015)., 10th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), 29 June-1 July, Bremen, Germany.

**26.** An energy-efficient virtual channel power-gating mechanism for on-chip networks. Mirhosseini Amirhossein, Sadrosadati Mohammad, Fakhrzadegan Ali, Modarressi Mehdi, Sarbazi-azad Hamid (2015)., Design, Automation & Test in Europe Conference (DATE), 9-13 March, paris, France.

**27.** A hybrid packet/circuit-switched router to accelerate memory access in NoC-based chip multiprocessors. Mazloumi Abbas, Modarressi Mehdi (2015)., Design, Automation & Test in Europe Conference (DATE), 9-13 March, paris, France.

**28.** An FPGA-Like Ultra Low-Power Network-On-Chip for Multicore Embedded Systems. Zaeemi Meisam, Modarressi Mehdi (2014)., The 11th. FPGAWORLD Conference, 9-11 September, Denmark.

**29.** A Reconfigurable NoC Topology for the Dark Silicon Era. Modarressi Mehdi, Sarbazi-azad Hamid (2014)., The 11th. FPGAWORLD Conference, 9-11 September, Denmark.

**30.** A Reconfigurable Network-on-chip for Heterogeneous Many-core CMPs in the Dark Silicon Era. Modarressi Mehdi, Sarbazi-azad Hamid (2014)., 25th IEEE International Conference on Application-specific Systems, Architectures and Processors, 18-21 June, Switzerland.

**31.** Power and Performance Efficient Partial Circuits in Packet-Switched Networks-on-Chip. Teimouri Nasibeh, Modarressi Mehdi, Sarbazi-azad Hamid (2013)., 2013 21st Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP), 1-4 March, Belfast, Northern Ireland.

**32.** A Game Theoretical Thermal–Aware Run–Time Task Synchronization Method for Multiprocessor Systems–on–Chip. Asgarieh Yashar, Khabazian Mohamed-h, Modarressi Mehdi, Sarbazi-azad Hamid (2012)., 15th. Euromicro conference on Digital System Design, 29-30 November, İzmir, Turkey.

**33.** A Game Theoretical Thermal - Aware Run - Time Task Synchronization Method for Multiprocessor Systems - on - Chip. Asgariye Yasgar, Khabazian Mohamed-hasan, Modarressi Mehdi, سربازی ازاد حمید (2012)., 15th Euromicro Conference on Digital System Design, 8 September-14 November, İzmir, Turkey.

**34.** Reconfigurable Cluster-Based Networks-on-Chip for Application-Specific MPSoCs. Modarressi Mehdi, H Sarbazi Azad (2012)., The 24th IEEE International Conference on Application-specific Systems, Architectures and Processors, 27 June-4 July, Lahe, Netherlands.

**35.** A Distributed Task Migration Scheme for Mesh-Based Chip-Multiprocessors. Yaghoubi Hossein, Modarressi Mehdi, سربازی ازاد حمید (2011)., Parallel and Distributed Computing, Applications and Technologies (PDCAT), 11 October-24 November, seoul, Korea.

**HONORS and AWARDS**

**ACADEMIC POSITIONS**

**Program committee member of The high-perfromance interconnect session of The International Conference on High Performance Computing & Simulation**
 2013-Present
**Program committee member of The high-perfromance interconnect (HPIN) session of The International Conference on High Performance Computing & Simulation**
 2014-Present
**PC member of the 23rd Euromicro Parallel, Distributed, and Network-Based Processing (PDP))**
 2015-Present
**PC member of the International Symposium on Real-Time and Embedded Systems and Technologies (RTEST)**
 2015-Present
**PC member of the 24th Euromicro Parallel, Distributed, and Network-Based Processing (PDP))**
 2016-Present
**Program committee member of the 4rd ACM International Workshop on Manycore Embedded Systems (in conjunction with ISCA))**
 2016-Present
**International Workshop on High Performance Interconnection Networks and Interconnects (HPINI 2016)**
 2016-Present
**PC member of the 25th Euromicro Parallel, Distributed, and Network-Based Processing (PDP))**
 2017-Present
**PC member of the 9th International Symposium on Computer Architecture and Digital Systems**
 2017-Present
**PC member of the 26th Euromicro Parallel, Distributed, and Network-Based Processing (PDP))**
 2018-Present
**PC member of the 2018 Euromicro Conference on Digital System Design (DSD)**
 2018-Present
**PC member of the Euromicro Parallel, Distributed, and Network-Based Processing (PDP)**
 2019-Present
**PC member of the 2019 Euromicro Conference on Digital System Design (DSD)**
 2019-Present
**TPC member of Euromicro digital system design conference**
 2020-Present
**TPC member of Euromicro parallel and distributed processing conference**
 2021-Present

**COURSES OFFERED**

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**LABORATORIES**