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**EDUCATION**

**Ph.D In Computer Engineering - Hardware**Sharif University of Technology 1997-2005  
**M.Sc In Computer Engineering - Hardware**University of Tehran 1995-1997  
**B.Sc In Computer Engineering - Hardware**Sharif University of Technology 1989-1995

**PUBLICATIONS**

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| **819** | **14** | **38** | **20** | **1** |
| Citations | h-Index | Article | Conference | Book |

***Articles***

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**2.** Adjoint recurrent neural network technique for nonlinear electronic component modeling. Naghibi Zohreh, Sadrossadat Sayed Alireza, Safari Saeed (2021)., INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, 50(4), 1119-1129.  
  
**3.** Recurrent neural networks models for analyzing single and multiple transient faults in combinational circuits. Farjaminezhad Rasoul, Safari Saeed, Eftekhari Moghadam Amir Masood (2021)., MICROELECTRONICS JOURNAL, 112(104993), 104993.  
  
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**5.** A digital hardware implementation of spiking neural networks with binary FORCE training. Akbarzadeh-sherbaf Kaveh, Safari Saeed, Vahabie Abdol-hossein (2020)., NEUROCOMPUTING, 412(1), 129-142.  
  
**6.** A reconfigurable real‐time neuromorphic hardware for spiking winner‐take‐all network. Abdoli Behrouz, Safari Saeed (2020)., INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, 48(12), 2141-2152.  
  
**7.** EREER: Energy-aware register file and execution unit using exploiting redundancy in GPGPUs. Yazdan Panah Alireza, Sajadimanesh Sohrab, Safari Saeed (2020)., MICROPROCESSORS AND MICROSYSTEMS, 77(1), 103176.  
  
**8.** SORT: Semi Online Reliable Task Mapping for Embedded Multi-Core Systems. Namazi Alireza, Safari Saeed, Mohammadi Siamak, Abdollahi Meisam (2019)., ACM Transactions on Modeling and Performance Evaluation of Computing Systems, 4(2), 1-25.  
  
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**12.** A memory-efficient canonical data structure for decimal floating point arithmetic systems modeling and verification. Mohammad saeed Jahangiry, Safari Saeed (2019)., Turkish Journal of Electrical Engineering and Computer Sciences, 27(1), 471-483.  
  
**13.** CMV: Clustered Majority Voting Reliability-Aware Task Scheduling for Multicore Real-Time Systems. Namazi Alireza, Safari Saeed, Mohammadi Siamak (2018)., IEEE TRANSACTIONS ON RELIABILITY, 1(1), 1-14.  
  
**14.** A Scalable FPGA Architecture for Randomly Connected Networks of Hodgkin-Huxley Neurons. Akbarzadeh-sherbaf Kaveh, Abdoli Behrouz, Safari Saeed, عبدالحسین وهابی (2018)., Frontiers in Neuroscience, 12(1), 1-14.  
  
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**18.** PVTA-aware approximate custom instruction extension technique: A cross-layer approach. Farahani Bahar, Safari Saeed, Shehatbakhsh Nader (2016)., MICROELECTRONICS RELIABILITY, 63(1), 267-277.  
  
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**1.** The VLSI Handbook. Safari Saeed (2006).

***Conferences***

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**2.** FPGA Implementation an Empirical Architecture for Online Real-Time Spike Sorting. Pakravan Payam, Safari Saeed, Abolghasemi Dehaqani Mohammadreza (2019)., Basic and clinical neuroscience, 18-20 December, Tehran, Iran.  
  
**3.** LRTM: Life-time and Reliability-aware Task Mapping Approach for Heterogeneous Multi-core Systems. Namazi Alireza, Abdollahi Meisam, Safari Saeed, Mohammadi Siamak, مسعود دانش طلب (2018)., 2018 11th International Workshop on Network on Chip Architectures (NoCArc), 20 October.  
  
**4.** LORAP: Low-Overhead Power and Reliability-Aware Task Mapping Based on Instruction Footprint for Real-Time Applications. Namazi Alireza, Abdollahi Meisam, Safari Saeed, Mohammadi Siamak (2017)., Euromicro Conference on Digital System Design (DSD), 30 August-1 September, Vienna, Austria.  
  
**5.** Reliability-Aware Task Scheduling using Clustered Replication for Multi-core Real-Time systems. Namazi Alireza, Abdollahi Meisam, Safari Saeed, Mohammadi Siamak, مسعود دانش طلب (2016)., 9th International Workshop on Network on Chip Architectures, 15-16 October.  
  
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**7.** SEERAD: A High Speed yet Energy-Efficient Roundingbased Approximate Divider. Zendegani Reza, Kamal Mehdi, Fayyazi Arash, Afzali Kousha Ali, Safari Saeed, مسعود پدرام (2016)., DATE, 14-18 March, Dresden, Germany.  
  
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**10.** Fault Tolerant Routing Algorithm in 3D Network on Chips. Maabi Somaieh, Safari Saeed (2014)., International Conference on Computers, 4-6 March, Tehran, Iran.  
  
**11.** Formal Verification and Debugging of Array Dividers with Auto-correction Mechanism. Haghbayan Hashem, Alizadehmalafeh Bijan, Behnam Payman, Safari Saeed (2014)., VLSI Design, 10-14 January, India.  
  
**12.** Capturing and mitigating the NBTI effect during the design flow for extensible processors. Kamal Mehdi, Afzali Kousha Ali, Safari Saeed, پدرام مسعود, Eghbalkhah Behzad (2013)., Design & Technology of Integrated Systems in Nanoscale Era (DTIS), 26-28 March, Abu Dhabi, United Arab Emirates.  
  
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**16.** An Efficient Relibaility Simulation Flow for Evaluating the Hot Carrier Injection Effect in CMOS VLSI Circuits. کمال مهدی, شی کینگ, پدرام مسعود, Afzali Kousha Ali, Safari Saeed (2012)., IEEE International Conference on Computer Design, 30 September-2 October, Montreal, Canada.  
  
**17.** Power Constraint Testing for Multi-Clock Domain SoCs Using Concurrent Hybrid BIST. حق بیان محمد هاشم, Safari Saeed, Navabi Shirazi Zainalabedin (2012)., DDECS 2012, 18-20 April, Tallinn, Estonia.  
  
**18.** A Link Failure Aware Routing Algorithm for Networks-on-Chip in Nano Technologies. Valinataj Mojtaba, Mohammadi Siamak, Safari Saeed, Plosila Juha (2009)., 9th International Conference on Nanotechnology IEEE Nano 2009, 26-30 July, Genoa, Italy.  
  
**19.** A Cost-Error Optimized Architecture for 9/7 Lifting Based Discrete Wavelet transform with Balanced Pipeline Stages. Aminlou Alireza, Refan Fatemeh, Hashemi Mahmoud Reza, Fatemi Omid, Safari Saeed (2009)., IEEE International on Acoustics Speech and Signal Processing 2009, 19-24 April, Taipei, Taiwan.  
  
**20.** Inherent Reliability Evaluation of Networks-on-Chip Based on Analytical Models. Valinataj Mojtaba, Mohammadi Siamak, Safari Saeed (2008)., International Symposium on System-on-Chip 2008-SOC08, 4-6 November, Tampere, Finland.

**HONORS and AWARDS**

**An Efficient Reliability Simulation Flow for Evaluating the Hot Carrier Injection Effect in CMOS VLSI Circuits** 2012, Tehran, Iran

**ACADEMIC POSITIONS**

**COURSES OFFERED**

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