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**EDUCATION**

**Ph.D In Computer Engineering - Hardware**Sharif University of Technology 1997-2005
**M.Sc In Computer Engineering - Hardware**University of Tehran 1995-1997
**B.Sc In Computer Engineering - Hardware**Sharif University of Technology 1989-1995

**PUBLICATIONS**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **819** | **14** | **38** | **20** | **1** |
| Citations | h-Index | Article | Conference | Book |

***Articles***

**1.** Compression of Deep Neural Networks based on quantized tensor decomposition to implement on reconfigurable hardware platforms. Nekooei Amirreza, Safari Saeed (2022)., NEURAL NETWORKS, 150(2022), 350-363.

**2.** Adjoint recurrent neural network technique for nonlinear electronic component modeling. Naghibi Zohreh, Sadrossadat Sayed Alireza, Safari Saeed (2021)., INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, 50(4), 1119-1129.

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**4.** A multiple-event propagation model in near-threshold combinational circuits using neural networks. Hajian Ali, Safari Saeed (2021)., Journal of Computational Electronics, 20(2), 1032-1042.

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**6.** A reconfigurable real‐time neuromorphic hardware for spiking winner‐take‐all network. Abdoli Behrouz, Safari Saeed (2020)., INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, 48(12), 2141-2152.

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**12.** A memory-efficient canonical data structure for decimal floating point arithmetic systems modeling and verification. Mohammad saeed Jahangiry, Safari Saeed (2019)., Turkish Journal of Electrical Engineering and Computer Sciences, 27(1), 471-483.

**13.** CMV: Clustered Majority Voting Reliability-Aware Task Scheduling for Multicore Real-Time Systems. Namazi Alireza, Safari Saeed, Mohammadi Siamak (2018)., IEEE TRANSACTIONS ON RELIABILITY, 1(1), 1-14.

**14.** A Scalable FPGA Architecture for Randomly Connected Networks of Hodgkin-Huxley Neurons. Akbarzadeh-sherbaf Kaveh, Abdoli Behrouz, Safari Saeed, عبدالحسین وهابی (2018)., Frontiers in Neuroscience, 12(1), 1-14.

**15.** Storage capacity for EDF–ASAP algorithm in energy-harvesting systems with periodic implicit deadline hard real-time tasks. Ghadaksaz Ehsan, Safari Saeed (2018)., JOURNAL OF SYSTEMS ARCHITECTURE, 89(1), 10-17.

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**38.** HW / SW Architecture for Soft - Error Cancellation in Real - Time Operating System. Mohammad Neishaburi, Mohammad Kakoee, Masood Daneshtalab, Safari Saeed (2007)., IEICE Electronics Express, 1(4), 755-761.

***Books***

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**2.** FPGA Implementation an Empirical Architecture for Online Real-Time Spike Sorting. Pakravan Payam, Safari Saeed, Abolghasemi Dehaqani Mohammadreza (2019)., Basic and clinical neuroscience, 18-20 December, Tehran, Iran.

**3.** LRTM: Life-time and Reliability-aware Task Mapping Approach for Heterogeneous Multi-core Systems. Namazi Alireza, Abdollahi Meisam, Safari Saeed, Mohammadi Siamak, مسعود دانش طلب (2018)., 2018 11th International Workshop on Network on Chip Architectures (NoCArc), 20 October.

**4.** LORAP: Low-Overhead Power and Reliability-Aware Task Mapping Based on Instruction Footprint for Real-Time Applications. Namazi Alireza, Abdollahi Meisam, Safari Saeed, Mohammadi Siamak (2017)., Euromicro Conference on Digital System Design (DSD), 30 August-1 September, Vienna, Austria.

**5.** Reliability-Aware Task Scheduling using Clustered Replication for Multi-core Real-Time systems. Namazi Alireza, Abdollahi Meisam, Safari Saeed, Mohammadi Siamak, مسعود دانش طلب (2016)., 9th International Workshop on Network on Chip Architectures, 15-16 October.

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**7.** SEERAD: A High Speed yet Energy-Efficient Roundingbased Approximate Divider. Zendegani Reza, Kamal Mehdi, Fayyazi Arash, Afzali Kousha Ali, Safari Saeed, مسعود پدرام (2016)., DATE, 14-18 March, Dresden, Germany.

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**9.** An Instance-based SER Analysis in the Presence of PVTA Variations. Farahani Bahareh, Safari Saeed (2014)., DFT, 1-3 October, Amsterdam, Netherlands.

**10.** Fault Tolerant Routing Algorithm in 3D Network on Chips. Maabi Somaieh, Safari Saeed (2014)., International Conference on Computers, 4-6 March, Tehran, Iran.

**11.** Formal Verification and Debugging of Array Dividers with Auto-correction Mechanism. Haghbayan Hashem, Alizadehmalafeh Bijan, Behnam Payman, Safari Saeed (2014)., VLSI Design, 10-14 January, India.

**12.** Capturing and mitigating the NBTI effect during the design flow for extensible processors. Kamal Mehdi, Afzali Kousha Ali, Safari Saeed, پدرام مسعود, Eghbalkhah Behzad (2013)., Design & Technology of Integrated Systems in Nanoscale Era (DTIS), 26-28 March, Abu Dhabi, United Arab Emirates.

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**14.** FPGA Implementation of a Cortical Network Based on the Hodgkin-Huxley Neuron Model. یقینی صفا, اصغریان ح, بختیاری ریحانه, Safari Saeed, Nili Ahmad Abadi Majid (2012)., ICONIP, 12-15 November, Doha, Qatar.

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**16.** An Efficient Relibaility Simulation Flow for Evaluating the Hot Carrier Injection Effect in CMOS VLSI Circuits. کمال مهدی, شی کینگ, پدرام مسعود, Afzali Kousha Ali, Safari Saeed (2012)., IEEE International Conference on Computer Design, 30 September-2 October, Montreal, Canada.

**17.** Power Constraint Testing for Multi-Clock Domain SoCs Using Concurrent Hybrid BIST. حق بیان محمد هاشم, Safari Saeed, Navabi Shirazi Zainalabedin (2012)., DDECS 2012, 18-20 April, Tallinn, Estonia.

**18.** A Link Failure Aware Routing Algorithm for Networks-on-Chip in Nano Technologies. Valinataj Mojtaba, Mohammadi Siamak, Safari Saeed, Plosila Juha (2009)., 9th International Conference on Nanotechnology IEEE Nano 2009, 26-30 July, Genoa, Italy.

**19.** A Cost-Error Optimized Architecture for 9/7 Lifting Based Discrete Wavelet transform with Balanced Pipeline Stages. Aminlou Alireza, Refan Fatemeh, Hashemi Mahmoud Reza, Fatemi Omid, Safari Saeed (2009)., IEEE International on Acoustics Speech and Signal Processing 2009, 19-24 April, Taipei, Taiwan.

**20.** Inherent Reliability Evaluation of Networks-on-Chip Based on Analytical Models. Valinataj Mojtaba, Mohammadi Siamak, Safari Saeed (2008)., International Symposium on System-on-Chip 2008-SOC08, 4-6 November, Tampere, Finland.

**HONORS and AWARDS**

**An Efficient Reliability Simulation Flow for Evaluating the Hot Carrier Injection Effect in CMOS VLSI Circuits** 2012, Tehran, Iran

**ACADEMIC POSITIONS**

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